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Question Paper Code : X 10311

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2020
Third Semester
Computer Science and Engineering
CS 8351 – DIGITAL PRINCIPLES AND SYSTEM DESIGN
(Common to Electronics and Telecommunication Engineering/
Information Technology)
(Regulations 2017)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. Reduce AB + (AC)′ + AB'C (AB + C).

2. A bulb in a staircase has two switches, one switch being at the ground floor and the other one at the first floor. The bulb can be turned ON and also can be turned OFF by any one of the switches irrespective of the state of the other switch. Which logic gate does the logic of switching of the bulb resembles ?

3. What is priority encoder ?

4. The output Y of a 2-bit comparator is logic 1 whenever the 2-bit input A is greater than the 2-bit input B. What is the number of combinations for which the output is logic 1 ?

5. How do you eliminate the race around condition in a JK flip-flop ?

6. How many flip-flops are required to build a binary counter that counts from 0 to 1023 ?

7. What are Hazards ?

8. What is state table ?

9. What are the advantages of static RAM and dynamic RAM ?

10. What is PAL ?

PART – B **(5×13=65 Marks)**

11. a) Given the Boolean function F = xy′z + x′y′z + w′xy + wx′y + wxy.

i) Obtain the truth table of the function. **(2)**

ii) Draw the logic diagram using the original Boolean expression. **(2)**

iii) Simplify the function to a minimum number of literals using Boolean algebra. **(3)**

iv) Obtain the truth table of the function from the simplified expression and show that it is the same as the one in part.(a). **(3)**

v) Draw the logic diagram from the simplified expression and compare the total number of gates with the diagram of part (b). **(3)**

(OR)

b) Consider,

F1 = xyz′ + wx′y′ + (x′ + z + w) (x′ + z + w′) + xyz + wx′y

F2 = xy + wx′ + x′ + z

i) Without using K-Map, show F1 can be simplified to F2 by algebraic means. **(7)**

ii) Implement F2 using NAND gates only. Assume all variables are available in both true and complement form. **(6)**

12. a) Design a combinational circuit with three inputs, x, y and z and three outputs, A, B and C. When the binary input is 0, 1, 2 or 3 the binary output is one greater than the input. When the binary input is 4, 5, 6 or 7, the binary output is one less than the input.

(OR)

b) Design a code converter that converts a decimal digit from ″8 4 – 2 – 1″ code to BCD.

13. a) Consider the following circuit involving three D-type flip-flops used in a certain type of counter configuration.

i) If at some instance prior to the occurrence of the clock edge, P, Q and R have a value 0, 1 and 0 respectively, what shall be the value of PQR after the clock edge ? **(7)**

ii) If all the flip-flops were reset to 0 at power on, what is the total number of distinct outputs (states) represented by PQR generated by the counter ? **(6)**

(OR)

b) A traffic signal cycles from GREEN to YELLOW, YELLOW to RED and RED to GREEN. In each cycle, GREEN is turned on for 70 seconds, YELLOW is turned on for 5 seconds and the RED is turned on for 75 seconds. This traffic light has to be implemented using a Finite State Machine (FSM). The only input to this FSM is a clock of 5 second period. What is the minimum number of flip-flops required to implement this FSM ? Explain in detail.

14. a) The state table of an asynchronous circuit with three SR latches is shown below. Reduce the number of states in the state table using implication table.

(OR)

b) An asynchronous sequential circuit is described by the following excitation and output functions

$Y = x_1 x_2' + (x_1 + x_2')y$

$Z = y$

i) Draw the logic diagram of the circuit. **(3)**

ii) Derive the transition table and output map. **(3)**

iii) Obtain a 2-state flow table. **(3)**

iv) Describe in words the behaviour of the circuit. **(4)**

15. a) A 12-bit Hamming code word containing 8 bits of data and 4 parity bits is read from memory. What was the original 8-bit data word that was written into memory if the 12-bit word read out is as follows ?

i) 000011101010

ii) 101110000110

iii) 101111110100

(OR)

b) List the PLA and PAL programming table for the BCD to excess-3 code convert whose Boolean function are simplified as w = A + BC + BD, x = B′C + B′D + BC′D, y = CD + C′D, z = D'.

PART – C **(1×15=15 Marks)**

16. a) Given the following Boolean function , F = xy'z + z'y'z + w'xy + wx'y + wxy

i) Draw a corresponding Karnaugh map of the function. **(5)**

ii) Give minterm and maxterm expressions. **(5)**

iii) Simplify the function and implement it by NAND gates only. **(5)**

(OR)

b) A sequential circuit has three flip-flops, A, B, C ; one input x and one output y. The state diagram is shown below. The circuit is designed by treating the unused states as don't care conditions. The final circuit must be analyzed to ensure that it is self-correcting (i.e., if the circuit enters in any of the unused states, after finite number of clock cycles it comes to a used state). Use JK flip-flops for the design.